ABSTRACT

A digital processor with a cache that provides fast and low power operation. The cache contains a tag array and a data array. The tag array indicates whether a value is stored in the cache for a particular external address. Access to the data array is necessary to determine the actual value. Access of the data array overlaps access to the tag array. Access to the data array includes a step in which the charge stored on column lines corresponding to multiple ways within the data array is altered based on information stored in the memory . This step occurs while the tag array is being operated. Access to the data array includes a second step of sensing one of the state of charge on a selected column line. Sensing occurs after the value has been read from the tag array and the value in the tag array is used to indicate which, if any way in the data array to sense. Processors using this approach quickly read information from the cache, but consume small amounts of power and are therefore well suited for use in cellular telephones and portable electronic devices.